Testing Circuit-Partitioned 3D IC Designs

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IEEE Computer Society Annual Symposium on VLSI
Tampa, Fl, 2009
http://arch.ece.gatech.edu/mars.html
3D Integration

- Multiple layers of silicon
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- Interconnected with TSVs
  - Etched through thinned wafers
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  - Architecture
    - Blocks split across layers
  - Circuit
    - Transistors split across layers
Motivation

![Graph showing the relationship between Single Layer Yield and Stack Yield for different layer counts (1 Layer, 2 Layers, 4 Layers, 8 Layers, 16 Layers). The graph demonstrates that as the number of layers increases, the single layer yield decreases.]
Motivation

The graph illustrates the relationship between single layer yield and stack yield for different numbers of layers. The x-axis represents the single layer yield, ranging from 100% to 80%, while the y-axis represents the stack yield, ranging from 100% to 0%. The graph shows that as the number of layers increases, the single layer yield and the stack yield decrease. For example, a single layer yield of 100% corresponds to a stack yield of 95% for 1 layer, 80% for 2 layers, 70% for 4 layers, 60% for 8 layers, and 50% for 16 layers.
Motivation

The graph illustrates the decrease in stack yield as the number of single layer yields decreases. The x-axis represents the single layer yield, ranging from 0% to 100%, and the y-axis represents the stack yield, ranging from 0% to 100%. The graph shows the following:

- The stack yield decreases from 100% to 95% as the single layer yield increases from 0% to 100% for 1 Layer.
- The stack yield decreases from 100% to 95% as the single layer yield increases from 0% to 100% for 2 Layers.
- The stack yield decreases from 100% to 90% as the single layer yield increases from 0% to 100% for 4 Layers.
- The stack yield decreases from 100% to 81% as the single layer yield increases from 0% to 100% for 8 Layers.
- The stack yield decreases from 100% to 66% as the single layer yield increases from 0% to 100% for 16 Layers.

Legend:
- Blue: 1 Layer
- Red: 2 Layers
- Orange: 4 Layers
- Green: 8 Layers
- Brown: 16 Layers
Previous Works – Results

Layer 1

Layer 2

<table>
<thead>
<tr>
<th></th>
<th>Scan Cell Size</th>
<th>75.8 μm²</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Inter-die Vias</td>
<td>2397</td>
</tr>
<tr>
<td></td>
<td>Scan Cell Count</td>
<td>4794</td>
</tr>
<tr>
<td></td>
<td>Two cells per via</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Area</td>
<td>0.363 mm²</td>
</tr>
<tr>
<td></td>
<td>Overhead</td>
<td>0.165%</td>
</tr>
</tbody>
</table>
Kogge-Stone Adder

- Binary summation tree
  - P and G signals represented by arrows
- Trades off hardware for reduced fan-out
Kogge-Stone Adder

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- Binary summation tree
  - P and G signals represented by arrows
- Trades off hardware for reduced fan-out
- In second stage, there are two disjoint sets of logic
  - These sets do not interact, yet they compete for wiring tracts
- Four sets at third level
Bit-Split Kogge-Stone Adder

- Bit-splitting separates disjoint logic sets across layers
  - For two layers, we get an even layer and an odd layer
Bit-Split Kogge-Stone Adder

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- TSVs shuffle P&G signals in first level of logic
Bit-Split Kogge-Stone Adder

- Bit-splitting separates disjoint logic sets across layers
  - For two layers, we get an even layer and an odd layer
- TSVs shuffle P&G signals in first level of logic
- Now the second and third stages are much less congested
Bit-Split Kogge-Stone Adder

- But now first stage is much more complex
Bit-Split Kogge-Stone Adder

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- Bit-splitting can be repeated
  - TSVs in first two levels
  - One-fourth the complexity in all other levels
Bit-Split Kogge-Stone Adder

- But now first stage is much more complex
- Bit-splitting can be repeated
  - TSVs in first two levels
  - One-fourth the complexity in all other levels
- Trading off TSVs for reduced complexity
Testing the Adder

- Few TSVs located near the edge of the circuit
  - Scan-based test acceptable
Testing the Adder

- Few TSVs located near the edge of the circuit
  - Scan-based test acceptable
- Add a scan-cell to each TSV
  - Two per adder column
- No observation cells required
  - Values generated in level one logic observable at adder POs
Many-Port Register File

- Many ports to allow parallel access to many entries
  - 20 or more in recent out-of-order processors
Many-Port Register File

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- Wiring in cell grows quadratically with port count
  - Required to make room for extra word- and bit-lines
Many-Port Register File

- Many ports to allow parallel access to many entries
  - 20 or more in recent out-of-order processors
- Wiring in cell grows quadratically with port count
  - Required to make room for extra word- and bit-lines
- This increases
  - Cell size
  - Word-line length
  - Bit-line length
- All of these slow circuit down
Port-Split Register File

- To fight quadratic growth, we split ports across layers
- This reduces
  - Cell size
  - Word-line length
  - Bit-line length
- A very big win for 3D
- But how do we test the top layer pre-bond
Memory Test

- Suk and Reddy's Test B
  - Write '0' to all cells
Memory Test

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  - Write '1' to a particular cell
Memory Test

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Memory Test

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  - Read written cell and neighbors

- This algorithm tests not only each cell's functionality but also bridging between neighboring cells

- Standard neighborhood
  - Four adjacent cells
Pre-bond Memory Test

- We can't write to cells
Pre-bond Memory Test

- We can't write to cells
- But we can write through them
Pre-bond Memory Test

- We can't write to cells
- But we can write through them
- Transmit test
  - Write
Pre-bond Memory Test

- We can't write to cells
- But we can write through them
- Transmit test
  - Write and read simultaneously
- Requires at least one write and one read port per layer
Experimental Setup

- **Design**
  - 3D layouts using the 3D Magic tool
  - DRC rules from MITLL 180nm process
  - Simulation with HSPICE
  - Lvl 49 transistor model

- **Adder Test**
  - Verilog models
    - Separate bottom, top, and integrated models for 3D adder
  - FlexTest for test modeling

- **RF Test**
  - Algorithm
64-Bit Planar KS Adder
64-Bit 3D KS Adder

Top Layer

Bottom Layer
## Kogge-Stone Comparison

<table>
<thead>
<tr>
<th></th>
<th>2D Adder</th>
<th>3D Adder</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (μm²)</td>
<td>35.4k</td>
<td>23.5k</td>
<td>66%</td>
</tr>
<tr>
<td>Footprint (μm²)</td>
<td>35.4k</td>
<td>11.8k</td>
<td>33%</td>
</tr>
<tr>
<td>Delay (ns)</td>
<td>7.46</td>
<td>6.08</td>
<td>82%</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>26.1</td>
<td>22.6</td>
<td>87%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Design</th>
<th>Pattern Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>2D Adder</td>
<td>313</td>
</tr>
<tr>
<td>3D Adder</td>
<td></td>
</tr>
<tr>
<td>Top</td>
<td>146</td>
</tr>
<tr>
<td>Bottom</td>
<td>145</td>
</tr>
<tr>
<td>Vias</td>
<td>10</td>
</tr>
<tr>
<td>Total</td>
<td>301</td>
</tr>
</tbody>
</table>
128-bit, 6-port Planar RF
128-bit, 6-port 3D RF
### Register File Comparison

<table>
<thead>
<tr>
<th></th>
<th>2D RF</th>
<th>3D RF</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Area (μm²)</strong></td>
<td>20.3k</td>
<td>12.5k</td>
<td>61%</td>
</tr>
<tr>
<td><strong>Footprint (μm²)</strong></td>
<td>20.3k</td>
<td>6.24k</td>
<td>31%</td>
</tr>
<tr>
<td><strong>Delay (ps)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read '0'</td>
<td>1401</td>
<td>1043</td>
<td>74%</td>
</tr>
<tr>
<td>Read '1'</td>
<td>1407</td>
<td>1050</td>
<td>75%</td>
</tr>
<tr>
<td>Write '0'</td>
<td>520</td>
<td>308</td>
<td>59%</td>
</tr>
<tr>
<td>Write '1'</td>
<td>1381</td>
<td>735</td>
<td>53%</td>
</tr>
<tr>
<td><strong>Energy (pJ)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read '0'</td>
<td>0.149</td>
<td>0.126</td>
<td>85%</td>
</tr>
<tr>
<td>Read '1'</td>
<td>0.149</td>
<td>0.127</td>
<td>85%</td>
</tr>
<tr>
<td>Write '0'</td>
<td>2.342</td>
<td>1.704</td>
<td>73%</td>
</tr>
<tr>
<td>Write '1'</td>
<td>2.342</td>
<td>1.710</td>
<td>73%</td>
</tr>
</tbody>
</table>
## Register File Comparison

<table>
<thead>
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<tbody>
<tr>
<td>2D RF</td>
<td>8192</td>
</tr>
<tr>
<td>3D RF</td>
<td></td>
</tr>
<tr>
<td>Top</td>
<td>256</td>
</tr>
<tr>
<td>Bottom</td>
<td>4096</td>
</tr>
<tr>
<td>Vias</td>
<td>512</td>
</tr>
<tr>
<td>Total</td>
<td>4864</td>
</tr>
</tbody>
</table>

### Test Access

<table>
<thead>
<tr>
<th></th>
<th>Transmit '0'</th>
<th>Transmit '1'</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay (ps)</td>
<td>1346</td>
<td>1744</td>
</tr>
<tr>
<td>Energy (pJ)</td>
<td>0.189</td>
<td>0.139</td>
</tr>
</tbody>
</table>
Conclusion

- 3D pre-bond circuit test can be done
- It can be done using straight-forward extensions to planar scan-based test
- Even circuit-partitioned designs can, in most cases, be tested with scan-chain test
- Some designs will require new test algorithms
- Complete 3D test is similar in cost to, and sometimes significantly less, planar test
Thank you!

http://arch.ece.gatech.edu/mars.html